Silicon Gate HCMOS Macrocell Array
LSI 5000 Series

PRELIMINARY
May 1982

General

The LSI 5000 series of silicon gate HCMOS arrays from LSI LOGIC CORPORATION is a high performance family of arrays, with complexity ranging from 880 to 6,000 gates, and maximum pin count ranging up to 180. The LSI 5000 series uses 3 micron HCMOS technology with 2 level metal interconnect, offers Schottky TTL speeds at CMOS power consumption, and is alternate sourced by Toshiba Corporation.

Features

- Implements user defined logic
- 880 to 6,000 gate complexity
- Up to 180 pin count
- Double level metal interconnect
- Schottky TTL speeds at 5V supply
- Proven silicon gate 3μ HCMOS technology
- Ceramic and plastic packages available
- Supported by LDS-I™ (LSI Development System)
- Supports 7400 SSI/MSI functions directly
- Full input/output TTL/CMOS compatibility

Product Outline

Part Number	Gate Complexity	Max I/O Pads(3)	Recommended Power Pads(3)	Max Pins	Metal Levels	Gate Length μ	Gate Speed nsec(1)		Supported by LDS-I™
							Typ	Max(2)	
LSI 5080	880	66	2-8	74	2	3	2.5	4.5	Yes
LSI 5140	1404	84	2-8	92	2	3	2.5	4.5	Yes
LSI 5220	2224	106	4-8	114	2	3	2.5	4.5	Yes
LSI 5320	3192	130	4-8	138	2	3	2.5	4.5	Yes
LSI 5420	4202	148	8-16	156	2	3	2.5	4.5	Yes
LSI 5600	6000	172	8-16	180	2	3	2.5	4.5	Yes

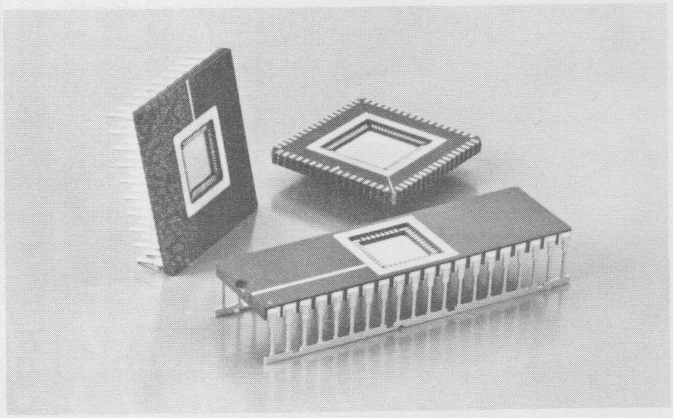
Notes:
1. Two input NAND gate, fanout 2, with 2 mm metal interconnect.
2. $T_A = 0$ to 70°C, $V_{DD} = 5V \pm 5\%$.
3. Additional V_{DD} and Ground pads may be required, reducing the available I/O, according to number of outputs used (see V_{DD} and Ground Requirements).

Packaging

The LSI 5000 series of HCMOS Macrocell arrays may be packaged in a variety of leadless and leaded chip carriers, pin grid array and dual in-line packages. Plastic packages are not available to full military temperature range. LSI LOGIC CORPORATION packaging Application Note A33 should be consulted for more details.

Recommended Packages(1)	
24-48 Lead	Dual In-Line
28-68 Lead	Leadless Chip Carrier
68-180 Lead	Pin Grid Array

Notes: 1. Subject to chip size limitation.



Examples of Recommended Packages

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Product Description

The LSI 5000 series of Macrocell arrays are manufactured using proven silicon gate oxide-isolated HCMOS process. Dual layer metal interconnect technology is used to implement the logic function.

The circuits are organized as arrays of cells as shown in Figure 1. The individual N and P channel transistors are configured into a variety of logic elements called Macrocells, using predefined metal interconnections. Currently there are approximately 60 Macrocells defined in the LSI 5000 series with additional elements being added on a regular basis. Figure 2 lists many of the Macrocells along with their complexity as measured by their number of equivalent 2 input nand gates.

A variety of input/output configurations are available.

- All I/O pads can be configured as inputs, outputs or bidirectional tristate.
- All I/O pads have active pullups and pulldowns available (typically 100k ohm).
- Any input may make use of TTL input level shifters to meet worst case TTL input specifications.
- All assigned outputs are capable of driving 4 LS TTL loads. Additional drive capability may be obtained by connecting output buffers in parallel to provide 8 or 12 LS load drive capability.

Many designers prefer to design with 7400 MSI logic functions. LSI Logic supports these higher level functions which are known as Macrofunctions. Most popular 7400 series functions are available to the user. Additional functions as required by the designer are added to the library on a regular basis. Macrofunctions are used at the logic design and simulation stage, then automatically simplified for layout. Tables 1 and 2, and the LSI LOGIC Application Note A31 contains more information on available Macrofunctions.

The LSI 5000 series of HCMOS Macrocell arrays are ideal for the replacement of LS/S TTL logic in medium and high speed systems. IC count can be reduced by factors of tens to hundreds depending on the density of the array used. Power requirements can be reduced by several orders of magnitude, reliability significantly enhanced and the total cost and size of the system similarly reduced.

The subject of TTL input buffering deserves further discussion. To meet the traditional TTL worst case V_{IH} of +2 volts, the input buffer may be used. Because the N device has a channel width eight times that of the P device, the effective threshold is lowered and +2 volts recognized as a logic 1. However the N and P impedance mismatch introduces substantial non-symmetrical delays. Fortunately a +2 volt V_{IH} minimum is not normally required in an actual system. When not sourcing significant DC current in the high state (as is normally the case) a LS/TTL output is one diode drop below V_{CC} or typically 4.2 volts. If a pullup to +5V is used (either on-chip or external resistor), the input rises to V_{DD}. The use of delay inducing TTL input shifters just to meet often unnecessary and overly conservative specifications should be reviewed with care prior to committing the final design.

The high density and low power dissipation of the LSI 5000 series of HCMOS Macrocell arrays make it ideal for high performance applications, where speed, space and power are at a premium.

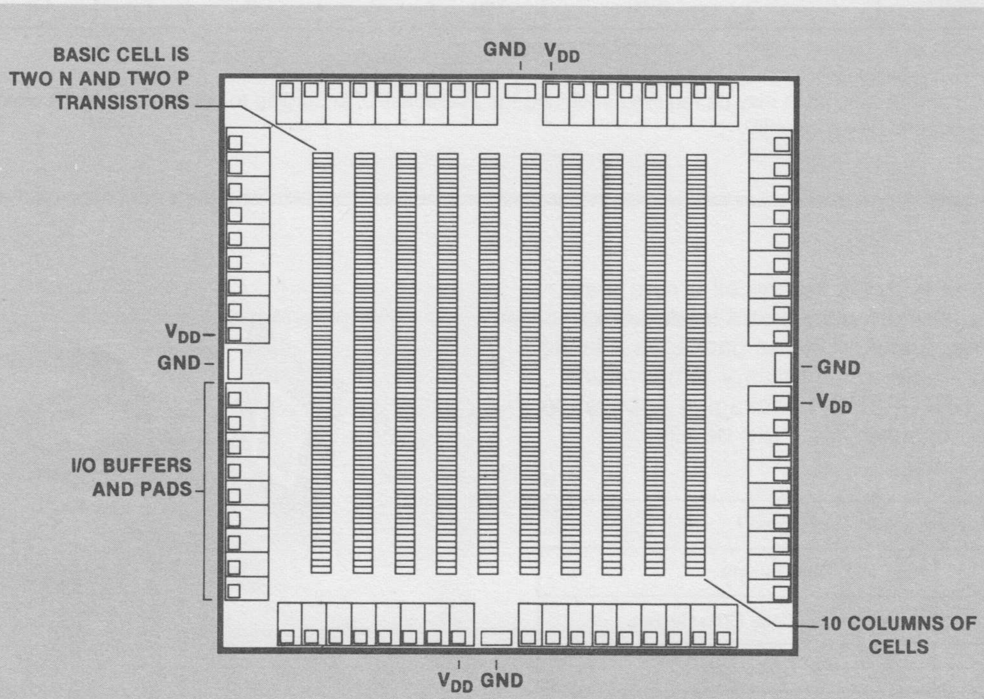


Figure 1. The 5080 Array Shown is Typical of the LSI 5000 Series Organization

Macrocell	Gate Equivalent
Transmission Gate	1
Transmission Gate Multiplexer	1
Inverter	1
Dual Inverter	1
Power Inverter	1
2 Input NAND	1
3 Input NAND	2
4 Input NAND	2
6 Input NAND	5
8 Input NAND	6
2 Input NOR	1
3 Input NOR	2
4 Input NOR	2
6 Input NOR	5
8 Input NOR	6
2 Input AND into 3 Input NOR	2
2 Dual Input AND's into 2 Input NOR	2
2 Input OR into 3 Input AND	2
2 Dual Input ORs into 2 Input NAND	2
Inverting Majority Gate	3
Exclusive OR	3
2 Input OR/NAND into 2 Input NAND	3
2 Input Equivalence	3

Macrocell	Gate Equivalent
2 Input AND/NOR into 2 Input NOR	3
Non-Inverting Internal Tri-State Buffer	4
Gated D Latch	3
Gated D Latch (Active Low Gate)	3
D Type Flip-Flop	5
D Type Flip-Flop with Direct Clear or Set	6
D Type Flip-Flop with Direct Clear and Set	7
JK Flip-Flop	8
JK Flip-Flop with Direct Clear or Set	9
JK Flip-Flop with Direct Clear and Set	10
Non-Inverting TTL to CMOS Clock Driver	5
Inverting Schmitt Trigger	5
Non-Inverting Output Buffer	2
Non-Inverting Output Buffer 2X Drive	4
Non-Inverting Output Buffer 3X Drive	6
Non-Inverting Tri-State Output Buffer	6
Non-Inverting Tri-State Output Buffer (Fast)	10
Pull-Up Resistor	one available on each I/O pin
Pull-Down Resistor	

Figure 2. Some Available Macrocells and Their Complexity Measured in Equivalent Gates

On-Chip Testing Aids

LSI LOGIC CORPORATION offers a full complement of on-chip testing techniques oriented towards designing testability and system diagnostics into the array. In particular, LSI LOGIC supports both level sensitive scan design and scan testing using either single or two phase clocks.

Scan testing, often associated with Level Sensitive Design, is in fact an independent concept which may be used with either one or two phase clocks. Scan testing simply involves the capability to serially shift the contents of all internal flip-flops off-chip in a test mode. This allows the contents of buried registers and counters to be easily examined. In addition, test patterns may be shifted into the array, initializing all internal memory elements to any desired state. Scan testing simplifies testing at the component level but more importantly, simplifies system diagnostics. If properly designed, entire boards of arrays may be put into test mode and all internal registers read out and analyzed, greatly reducing repair time.

To provide scan testing of the array it is necessary to add three I/O pins: Test Input, Test Output and Test Enable. Additionally, all flip-flops and latches must have multiplexed inputs so that they may be connected as shift registers in the test mode. For those using the classic IBM LSSD, two latch configurations, LS1 and LS2 are available. The LS1 is a D latch with two independently gated D inputs. The LS2 is an LS1 with another gated latch to store its output.

For those desiring to use scan testing with the more traditional single phase clocks, a family of Macrocells and Macrofunctions is available. The family is a superset of the flip-flop cells and Macrofunctions containing flip-flops. Each member of the family has two additional inputs, test input (TI) and test enable (TE). By connecting these family members together, all flip-flops can become a shift register when the test input is enabled (Figure 3). All that is required to select the scan logic elements is to add an ''S suffix'' to any flip-flop or MSI element containing flip-flops. In the TEGAS V netlist two additional entries corresponding to test select and test source are inserted.

Because of the ease of use of our scan testing capability, arrays may be designed in the conventional fashion and a scan testing capability easily added with a few statements. The overhead for scan testing, as compared to a non-scan test design, is three I/O pins and 10 to 20% extra gates, depending on the design.

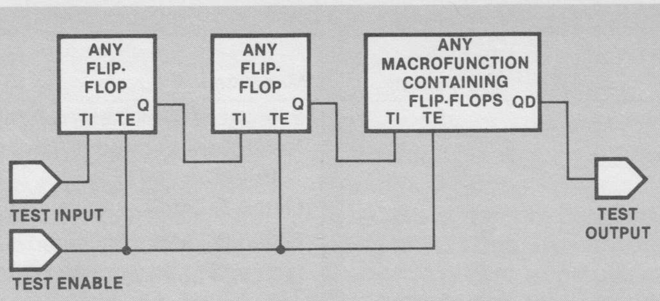


Figure 3. Scan Testing May be Added Easily to Any Macrocell or Macrofunction

Propagation Delays

Propagation delays of LSI 5000 Series HCMOS array logic elements are a function of a number of factors:

- Fanout
- Interconnection routing
- Junction temperature
- Supply voltage
- Processing tolerance
- Input transition time
- Input signal polarity

Once a design has been entered into the LDS I Development System, the LDPS delay path program provides listings of these delays. Prior to layout, the values are based on estimated interconnections; after layout the program is rerun and final delay values listed, based on actual interconnections.

Prior to the availability of the network in computer format, approximate delay calculations may be used. This may be done as follows:

The Figures 10 and 11 list typical delays for many common array logic elements (Macrocells). The delays of Figure 11 include the effect of interconnections based on an assumed interconnection length of one millimeter per fanout. Delays for greater fanout or other logic elements may be extrapolated from the table, as required.

The effect of temperature (K_T) may be estimated using Figure 4. The maximum junction temperature (which in CMOS is usually quite close to the ambient temperature) will determine a propagation delay multiplier. Similarly, the effect of supply voltage variation (K_V) is determined by use of Figure 5. The maximum effects of process variation (K_P) is calculated to be $\pm 40\%$; therefore, a factor of 1.4 should be used to estimate maximum propagation delay.

The maximum propagation delay is therefore:

$$T_{MAX} = K_P \cdot K_T \cdot K_V \, (T_{TYP})$$

Output buffer delays are shown in Figures 6 and 7 for driving TTL and CMOS. The difference in the two cases is caused by the different input thresholds of the driven elements, 1.3 volts for TTL, 2.5 volts for CMOS. CMOS inputs which use input level shifters will exhibit the same 1.3 volt threshold as TTL. As with internal gates, the worst case delays are calculated using the K_P K_T K_V multiplier factors, defined above.

Example

A simple example will illustrate the technique. The circuit of Figure 9 must operate over 0 to 70°C temperature and 4.75 to 5.25 volt power supply variation. Using Figures 4 and 5 and the 1.4 process multiplier, we determine that the worst case maximum delay will be $1.4 \times 1.16 \times 1.07 = 1.74$ times that of the typical delay.

The AO2 AND-NOR gate, shown in Figure 8, illustrates the advantage of the CMOS implementation. Two levels of gating are achieved with a single inversion. The AO2 drives a BTS1 three state buffer directly. The BTS1 drives off chip, through a pc board, and on to another array using a TLCH input level shifter. The total capacity of the output, interconnect, and input is 35 pF. The TLCH drives the D input of a FD2 D flip-flop plus two other loads. The buffer characteristics of Figure 6 and the delays of Figure 11 were consulted and the positive and negative going delays tabulated in Figure 9. Two values were unavailable directly and were estimated. The FD1 flip-flop delays are listed up to afanout of four; in this usage the fanout was 5. Extrapolating from data shown, delays of 13.3 ns and 8.9 were assumed.

The total clock to clock delay is 31.7 ns typical, 55.2 ns worst case. The LDPS program in the LDS-I may be used to obtain more accurate delays, after the logic has been simulated.

As a comparison, 74LS TTL data was taken from the TI TTL Data Book (Second Edition).

	74LS74A flip-flop Clock to output delay	74LS51 AND-OR-INVERT gate delay	74LS74A Set up
T_{PLH}	25	20	not given
T_{PHL}	40	20	not given

Unfortunately no exact comparison could be made because of the unavailability of 74LS74A set up time. In addition, no data was readily available on effects of temperature and supply voltage variation for these TTL devices. Where comparisons could be made, the 5000 Series D flip-flop and AO2 AND-OR-INVERT gate were better than twice as fast as 74LS.

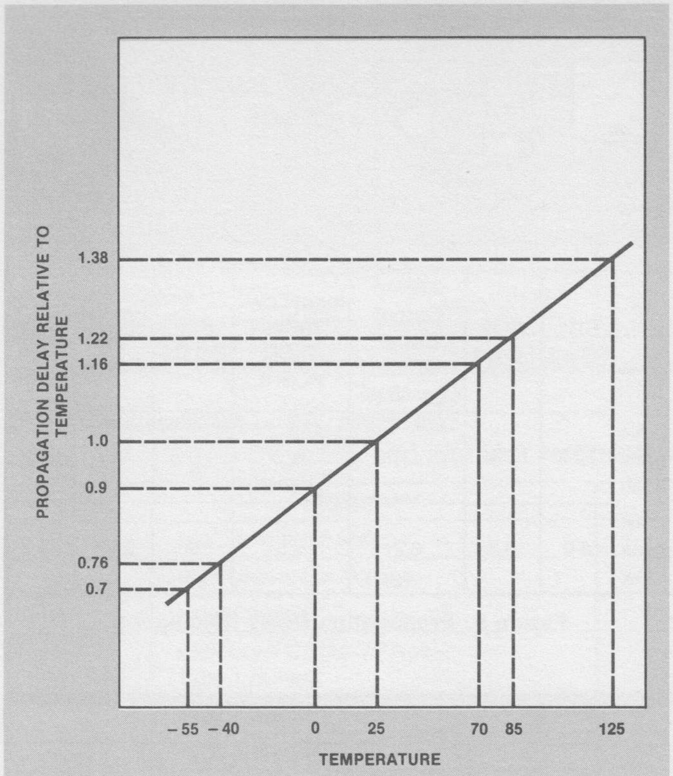


Figure 4. CMOS Propagation Delay as a Function of Temperature

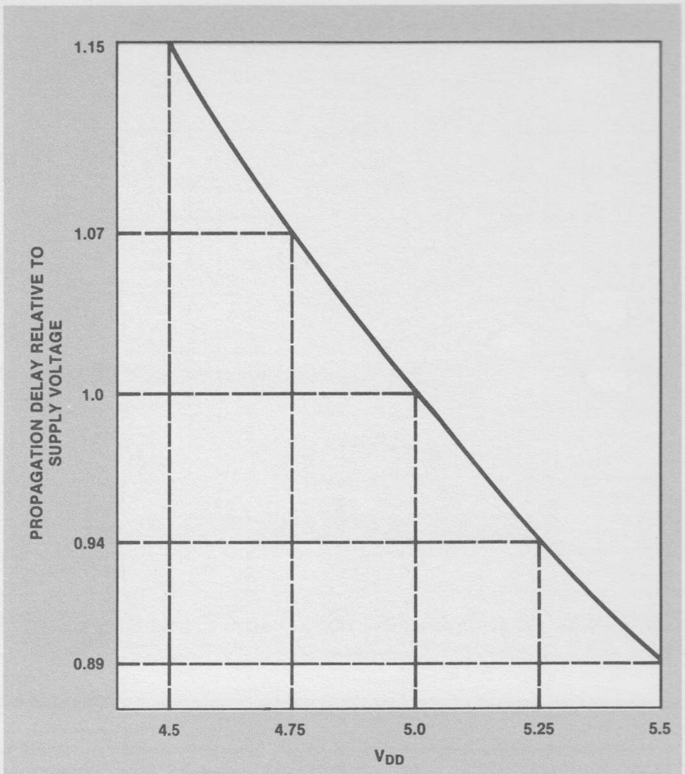


Figure 5. CMOS Propagation Delay as a Function of Supply Voltage

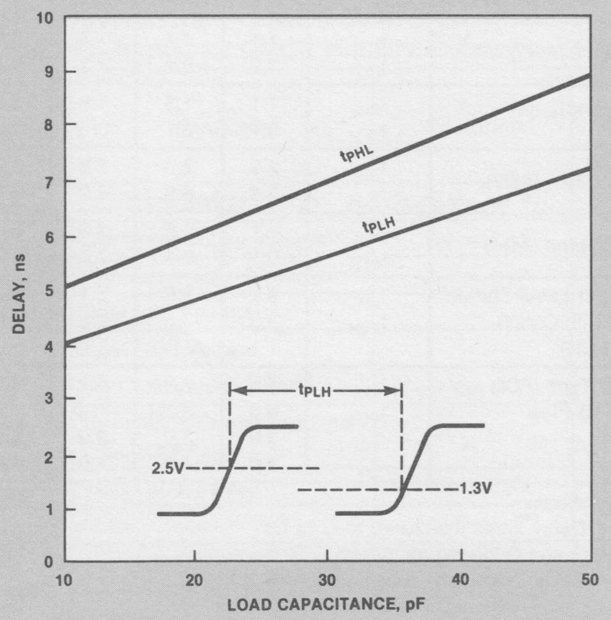


Figure 6. BTS1 TTL Driver Delay as a Function of Load Capacitance. $V_{DD} = 5V$, $T_A = 25°C$.

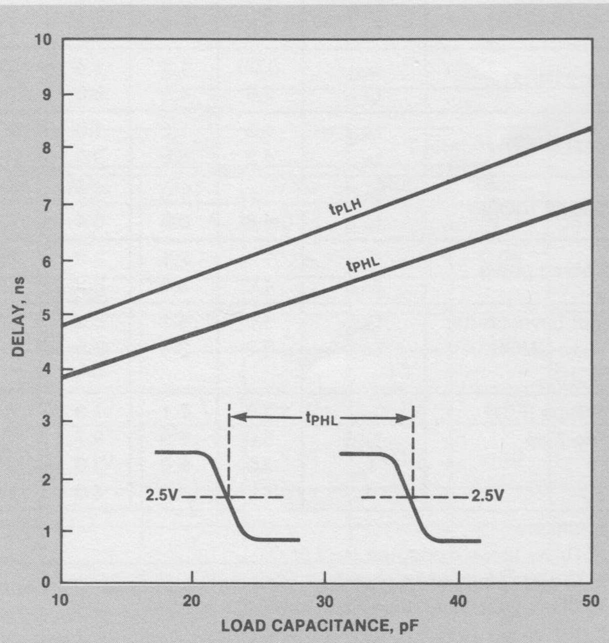


Figure 7. BTS6 CMOS Driver Delay as a Function of Load Capacitance. $V_{DD} = 5V$, $T_A = 25°C$.

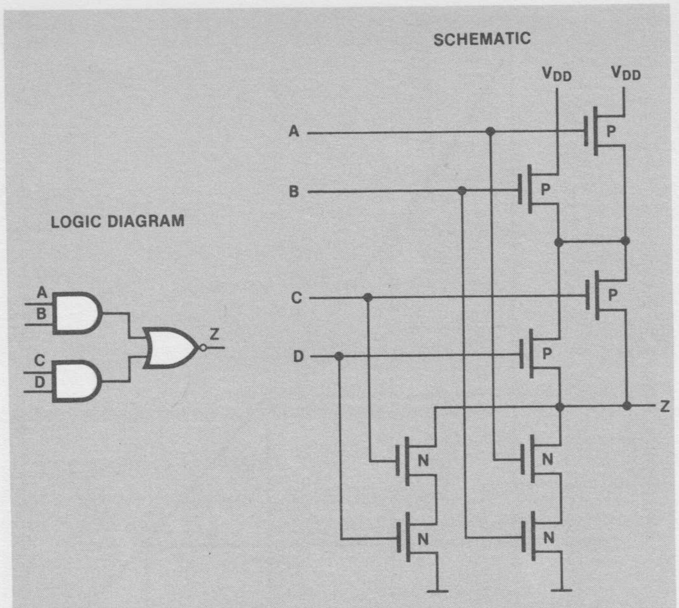
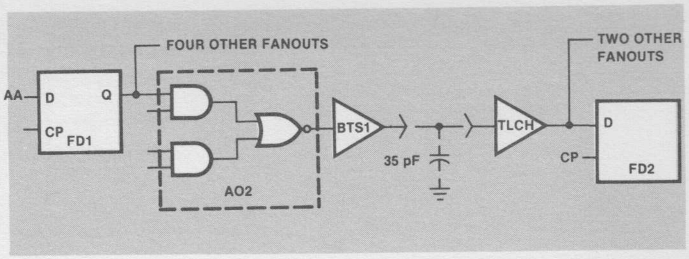


Figure 8. AO2 Macrocell Logic Diagram and Schematic



	FD1 FO = 5	AO2 FO = 1	3-State Output Buffer BTSI $C_L = 35$ pF	Input Level Shifter TLCH FO = 3	FD2 Set Up	Typical Path Delay	Worst Case Path Delay
AA goes high	13.3	1.9	7.4	6.1	3	31.7	55.2
AA goes low	8.9	5.3	6.2	3.8	3	27.2	47.3

Figure 9. Propagation Delay Calculation

Macrocell	Output Transition	FO = 1	FO = 2	FO = 3	FO = 4
Inverter (IVD)	t_{PHL} t_{PLH}	0.77 1.3	1.1 1.9	1.3 2.7	1.5 3.6
Power Inverter (IVP)	t_{PHL} t_{PLH}	0.59 1.1	0.77 1.3	0.92 1.6	1.1 1.9
Nand 2 (ND2)	t_{PHL} t_{PLH}	1.1 1.7	1.5 2.3	1.9 3.1	2.3 4.0
Nand 3 (ND3)	t_{PHL} t_{PLH}	1.7 2.0	2.3 2.7	2.8 3.4	3.4 4.2
Nor 2 (NR2)	t_{PHL} t_{PLH}	0.90 2.6	1.2 4.0	1.4 5.6	1.6 7.3
Nor 3 (NR3)	t_{PHL} t_{PLH}	1.0 4.3	1.2 6.6	1.5 9.0	1.7 11.2
And-Nor (AO2)	t_{PHL} t_{PLH}	1.7 4.8	1.9 5.6	2.2 6.4	2.4 7.2
Or-Nand (AO4)	t_{PHL} t_{PLH}	1.9 4.6	2.1 5.5	2.3 6.2	2.6 7.0
Input Level Shifter TTL to CMOS (TLCH)	t_{PHL} t_{PLH}	5.6 3.3	5.7 3.4	5.9 3.6	6.0 3.7
*D-Type (FDI) Flip Flop	t_{PHL} t_{PLH} t_{su} t_h	7.0 6.0 3.0 4.0	7.1 8.9 3.0 4.0	7.3 9.7 3.0 4.0	7.5 10.6 3.0 4.0

*Conditions:
- Delay times measured to Q or $\overline{Q}$.
- Q and $\overline{Q}$ loaded as shown.
- Clock Definition: Rise/Fall Time = 2.3 nsec
  Pulse Width = 4 nsec

Figure 10. Typical Propagation Delay (ns) with No Metal Interconnection. $V_{DD} = 5V$, T = 25°C.

Macrocell	Output Transition	FO = 1 1 mm Metal	FO = 2 2 mm Metal	FO = 3 3 mm Metal	FO = 4 4 mm Metal
Inverter (IVD)	t_{PHL} t_{PLH}	0.94 1.6	1.3 2.5	1.6 3.6	2.0 4.6
Power Inverter (IVP)	t_{PHL} t_{PLH}	0.70 1.2	0.94 1.6	1.1 2.0	1.3 2.5
Nand 2 (ND2)	t_{PHL} t_{PLH}	1.4 2.0	2.0 3.0	2.5 4.0	3.1 5.1
Nand 3 (ND3)	t_{PHL} t_{PLH}	2.0 2.3	2.9 3.3	3.7 4.3	4.5 5.3
Nor 2 (NR2)	t_{PHL} t_{PLH}	1.1 3.2	1.4 5.1	1.8 7.3	2.1 9.4
Nor 3 (NR3)	t_{PHL} t_{PLH}	1.1 5.1	1.5 8.1	1.9 11.2	2.2 14.2
And-Nor (AO2)	t_{PHL} t_{PLH}	1.9 5.3	2.3 6.5	2.8 8.0	3.2 9.1
Or-Nand (AO4)	t_{PHL} t_{PLH}	2.1 5.1	2.5 6.4	3.0 7.7	3.4 8.8
Input Level Shifter TTL to CMOS (TLCH)	t_{PHL} t_{PLH}	5.7 3.3	5.9 3.6	6.1 3.8	6.3 4.0
*D-Type (FDI) Flip Flop	t_{PHL} t_{PLH} t_{su} t_h	7.5 6.6 3.0 4.0	7.9 10.0 3.0 4.0	8.2 11.0 3.0 4.0	8.5 12.1 3.0 4.0

*Conditions:
- Delay times measured to Q or $\overline{Q}$.
- Q and $\overline{Q}$ loaded as shown.
- Clock Definition: Rise/Fall Time = 2.3 nsec
  Pulse Width = 4 nsec

Figure 11. Typical Propagation Delay (ns) with Metal Interconnection. $V_{DD} = 5V$, T = 25°C.

Operating Characteristics

Absolute Maximum Ratings (Referenced to V_{SS})

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	-0.3 to $+7$	V
Input Voltage	V_I	-0.3 to $V_{DD}+0.3$	V
DC Input Current(8)	I_I	±10	mA
Storage Temperature Range (Ceramic)	T_{STG}	-65 to $+150$	°C
Storage Temperature Range (Plastic)	T_{STG}	-40 to $+125$	°C

Recommended Operating Conditions

Parameter	Symbol	Limits	Unit
DC Supply Voltage	V_{DD}	$+3$ to $+6$	V
Operating Ambient Temperature Range			
Military	T_A	-55 to $+125$	°C
Industrial Range	T_A	-40 to $+85$	°C
Commercial Range	T_A	0 to $+70$	°C

DC Characteristics — TTL Interface

Specified at $V_{DD} = 5V \pm 5\%$ and ambient temperature over the specified temperature range[1]

Symbol	Parameter	Condition	Min.	Typ.	Max.	Unit
V_{IL}	Low Level Input Voltage				0.8(3)	V
V_{IH}	High Level Input Voltage		2(3)			V
I_{IN}	Input Current(4)	$V_{IN} = V_{SS}$ or V_{DD}	-10	±1	10	µA
V_{OH}	High Level Output Voltage Type 1 Buffers	$I_{OH} = -1.5$ mA	2.4	4.5		V
	Type 2 Buffers	$I_{OH} = -3$ mA				
	Type 3 Buffers	$I_{OH} = -4.5$ mA				
V_{OL}	Low Level Output Voltage(2) Type 1 Buffers	$I_{OL} = 1.6$ mA		0.2	0.4	V
	Type 2 Buffers	$I_{OL} = 3.2$ mA				
	Type 3 Buffers	$I_{OL} = 4.8$ mA				
I_{OZ}	Three-State Output Leakage Current	$V_{OH} = V_{SS}$ or V_{DD}	-10	±1	10	µA
I_{OS}	Output Short Circuit Current(5)	$V_{CC} = \max$, $V_O = V_{CC}$	25		90	mA
		$V_{CC} = \max$, $V_O = 0$	-7		-28	mA

DC Characteristics — CMOS Interface

(EIA/JEDEC format for CMOS industry B specifications, $V_{DD} = 5V$)

Symbol	Parameter	Condition	Limits							Unit
			T Low(1)		25°C			T High(1)		
			Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
I_{DD}	Quiescent Supply Current	$V_{IN} = V_{DD}$ or V_{SS}		10^{-2}		10^{-4}	10^{-2}		10^{-2}	µA/gate
V_{OL}	Low Level Output Voltage	$\lvert I_O \rvert \le 1$ µA		0.05			0.05		0.05	V
V_{OH}	High Level Output Voltage	$\lvert I_O \rvert \le 1$ µA	4.95		4.95			4.95		V
V_{IL}	Input Low Voltage			1.5			1.5		1.5	V
V_{IH}	Input High Voltage		3.5		3.5			3.5		V
I_{IN}	Input Leakage Current(4)	$V_{IN} = V_{SS}$ or V_{DD}	-10	$+10$	-10	±1	$+10$	-10	$+10$	µA
I_{OZ}	Three-State Output Leakage Current(6)	$V_o = V_{SS}$ or V_{DD}	-10	$+10$	-10	±1	$+10$	-10	$+10$	µA
C_{IN}	Input Capacitance	Any Input(6)				5				pF
C_{OUT}	Output Capacitance	Any Output(7)				7				pF

Notes:

1. Military temperature range is -55°C to $+125$°C (ceramic packages only).
   Industrial temperature range is -40°C to $+85$°C.
   Commercial temperature range is 0°C to $+70$°C.
2. There may be limitations on maximum current when many outputs are low simultaneously.
3. Using a TTL input buffer (see Product Description, page 2).
4. For inputs not having on-chip pull-up or pull-down resistors.
5. Not more than one output may be shorted at a time for a maximum duration of one second.
6. Not applicable to assigned bi-directional buffer (excluding package).
7. Output using single buffer structure (excluding package).
8. Not more than one second duration.

Power Consumption Calculation

Power dissipation in CMOS circuits is made up of three basic elements. The first and most important is the charging and discharging of circuit capacitances which makes up the major portion of AC power dissipation, and contributes in excess of 90% of total power dissipated. The second is due to overlap currents when the P and N transistors are switching from the high to the low state or vice versa. This contributes less than 10% of the power dissipated and occurs for the transition period when $V_{TH(N)} < V_{IN} < V_{DD} - V_{TH(P)}$. The third element of power dissipation is due to leakages. These form DC power dissipation and are essentially negligible (few μW).

The charging of a capacitor C to a voltage V through a P channel device builds up a charge CV and stores energy $CV \times V = CV^2$ in the capacitance. This energy is later discharged through an N transistor in the CMOS P-N pair. When such switching takes place at a frequency f, the resulting power dissipated in the CMOS circuit is equivalent to $P = CV^2 f$.

The power consumption for a specific application may be estimated by calculation, based on the conditions being used. While the calculation makes certain assumptions, it will adequately establish the power consumption for the purpose of system and power supply design considerations. The following examples are used to illustrate applications with conditions indicated.

Parameter	Part Type	
	LSI 5220	LSI 5600
No. of available gates	2224	6000
No. of gates utilized (70%)	1550	4200
No. switching each cycle (15%)	232	630
No. of outputs utilized	40	80
Output load Capacitance (pF)	45	45
No. switching each cycle (20%)	8	16
Supply Voltage (V)	5	5
Core dissipation per MHz (mW)	4.7	12.6
Output buffer dissipation per MHz (mW)	9.0	18.0
Total dissipation per MHz (mW)	13.7	30.6
At 10 MHz clock speed, total dissipation (mW)	137	306
At 25 MHz clock speed, total dissipation (mW)	343	765

Figure 12. Power Calculation Examples

V_{DD} and Ground Requirements

The design of the LSI 5000 series incorporates the minimum number of V_{DD} and ground pads that are required for a high input, low output pin count application. Many applications will require additional pad sites to be dedicated to V_{PP} or ground, or both, for operation within specification. The exact number of additional sites will be determined and set during the design of the array. As a guideline, it can be assumed that an output pad may not be more than 8 pads distant from a V_{DD} or ground. The following are example extreme cases where additional power pads are needed.

More Desirable	I	G	O	O	O	O	O	O	O	O	V	O	O	O	O	O	O	O	O	G	I
Less Desirable	I	V	O	O	O	O	O	O	O	O	G	O	O	O	O	O	O	O	O	V	I

Product Options Available

The LSI 5000 series is offered in a variety of operating temperature ranges and packages. Devices are specified over the full MIL temperature range in ceramic packages only.

- Military operating temperature range:
  −55°C to +125°C
- Industrial operating temperature range:
  −40°C to +85°C
- Commercial operating temperature range:
  0°C to +70°C
- MIL-STD-883 Level B and C Screening
- A wide variety of packages are available. Packaging Application Note A33 should be consulted for more information. Unpackaged die are also available, on special request.

Development Support and Interface

The LDS-I (LSI Development System I) is used for logic simulation, design verification, test pattern generation, layout and mask design. The desired logic function is entered into the system and the design electronically breadboarded using the LDS-I logic simulation and delay path analysis programs. The simulated input patterns are checked for completeness, and other tests added until the final test patterns are completed. The personality masks may then be designed using the LDS-I interactive/automatic placement and routing program. For more details see the LDS-I Product Description available from LSI LOGIC CORPORATION, or representative.

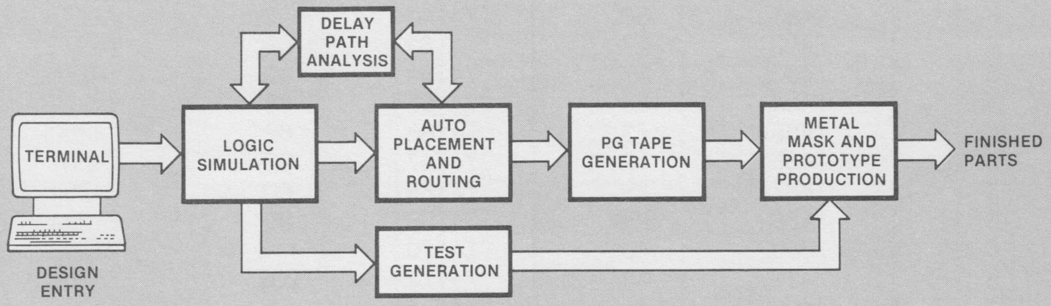


Figure 13. LDS-I Functional Outline

Trademarks

LDS-I is a trademark of LSI LOGIC CORPORATION.
TEGAS is a trademark of COMSAT GENERAL INTEGRATED SYSTEMS.
PAL is a trademark of MONOLITHIC MEMORIES INCORPORATED.

Estimating Equivalent Gate Complexity

One of the first tasks in converting your logic function into a logic array is to estimate its logic complexity. While no industry wide standard for logic complexity exists, most measure it in terms of "equivalent gates." These elements, typically two-input gates, may be used to implement more complex gates, flip-flops and on up to complex counters, shift registers and multiplexers, etc. Tables 1 and 2 list the approximate equivalent CMOS 2 input nand gate count of many common SSI and MSI functions.

Equivalent Gates for 7400 and 4000B Packages — These are approximate gate equivalent figures for 7400 and 4000B series packages, i.e. a 7400 quad two-input nand gate package is four equivalent gates. Unused portions of these functions may be deleted with a commensurate savings in gates. Off-chip output buffers and input level shifters are not included and must be added separately.

Non-logic 7400 and 4000B functions such as linear circuits and large memories are not included.

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.
7400	4	7470	16	74152	24	74253	40
7401	4	7471	15	74153	27	74257	36
7402	4	7472	14	74154	33	74258	34
7403	4	7473	20	74155	21	74259	48
7404	4	7474	15	74156	21	74260	6
7405	3	7475	14	74157	22	74261	58
7406	3	7476	20	74158	23	74265	7
7407	6	7477	14	74159	18	74266	10
7408	6	7478	20	74160	68	74273	50
7409	6	7480	17	74161	68	74274	70
7410	6	7481	80	74162	68	74275	70
7411	8	7482	27	74163	68	74276	40
7412	6	7483	57	74164	43	74278	34
7413	14	7484	80	74165	85	74279	10
7414	30	7485	73	74166	62	74280	24
7415	8	7486	12	74167	52	74281	170
7416	3	7487	19	74168	80	74283	59
7417	6	7489	320	74169	80	74284	58
7420	6	7490	40	74170	116	74285	58
7421	5	7491	43	74172	205	74289	280
7422	4	7492	41	74173	56	74290	48
7423	6	7493	41	74174	37	74293	45
7425	6	7494	42	74175	25	74295	57
7426	4	7495	42	74176	42	74298	32
7427	6	7496	44	74177	41	74299	188
7428	4	7497	120	74178	56	74323	188
7430	6	7498	33	74179	56	74348	64
7432	4	7499	46	74180	20	74351	124
7433	4	74100	18	74181	100	74352	26
7437	4	74102	14	74182	30	74353	39
7438	4	74103	20	74183	16	74362	44
7440	4	74106	20	74184	100	74363	28
7442	29	74107	20	74185	100	74364	48
7443	29	74108	20	74190	80	74365	37
7444	29	74109	21	74191	76	74366	40
7445	29	74110	14	74192	62	74367	37
7446	45	74111	20	74193	58	74368	40
7447	45	74116	26	74194	70	74373	58
7448	45	74120	15	74195	46	74374	74
7449	45	74135	24	74196	42	74375	16
7450	6	74136	12	74197	41	74376	40
7451	5	74138	23	74198	92	74377	48
7452	8	74139	20	74199	85	74378	34
7453	7	74141	16	74225	450	74379	24
7454	7	74142	90	74226	116	74381	150
7455	6	74143	45	74245	83	74386	12
7460	6	74144	98	74246	51	74390	86
7461	6	74145	24	74247	51	74393	80
7462	9	74147	35	74248	51	74395	50
7464	8	74148	35	74249	51	74398	22
7465	8	74150	60	74251	37	74399	22
		74151	24			74670	144

Table 1. 7400 Equivalent Gate Count for HCMOS Logic Arrays

Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.	Part No.	Gate Equiv.
4000	5	4028	22	4077	12	4175	25	4521	123
4001	4	4029	68	4078	4	4192	60	4522	44
4002	4	4030	12	4081	4	4193	56	4526	47
4006	108	4032	68	4082	4	4273	50	4530	16
4007	2	4034	110	4089	84	4373	58	4531	36
4008	32	4035	48	4093	32	4374	74	4532	39
4009	5	4038	74	4094	86	4375	14	4534	190
4010	5	4040	74	4099	64	4386	12	4539	24
4011	4	4041	4	4106	30	4501	6	4554	40
4012	4	4042	12	4107	18	4504	33	4555	22
4013	10	4043	20	4138	20	4505	271	4556	22
4014	43	4044	20	4139	10	4506	19	4558	65
4015	62	4051	6	4153	32	4508	24	4560	78
4017	45	4068	4	4155	22	4510	94	4580	187
4018	52	4069	3	4157	24	4511	136	4581	100
4019	12	4070	12	4158	24	4512	31	4582	31
4020	40	4071	6	4160	64	4514	69	4583	23
4021	43	4072	4	4162	64	4515	69	4584	30
4022	35	4073	8	4163	64	4516	66	4585	35
4024	44	4074	14	4164	51	4518	26	4597	103
4026	65	4075	8	4166	84	4519	28	4598	74
4027	20	4076	41	4174	38	4520	54	4599	42

Table 2. 4000B Equivalent Gate Count for HCMOS Logic Arrays

Converting PAL/FPLA Designs to Gate Arrays

Field programmable logic is a popular technology that is used to achieve higher levels of integration than is possible with standard 7400 series SSI/MSI functions. Typically between 5–12 standard SSI/MSI functions can be implemented on a single programmable logic circuit. These circuits are known by generic names such as PAL (Programmable Array Logic), FPLA (Field Programmable Logic Array) and FPLS (Field Programmable Logic Sequencer).

The function of a PLA may be implemented as a portion of a logic array with a commensurate cost savings. The conversion may take into account a number of factors.

- The original PLA program may have been generated from boolean expressions. These expressions may also be used to implement a gate solution.
- For higher speeds, the designer may wish to implement in the prime implicant form and optimize propagation delays.
- In many PLA designs all 8 or 10 outputs may be used simply because they were available. Some outputs may be more economically implemented in other ways.
- Most PLA designs only use about 50% of available minterms because of I/O pincount limitations. A good rule of thumb is to assume an average PLA design is about 200 gate complexity. Many designs use less than 200. Actual details of the logic would be required to come up with a final equivalent gate count.

Table 3 summarizes popular PLAs and the maximum and average logic complexity.

Part Type	Array Inputs	Outputs	Product Terms	Output Registers/ Tri-State Buffers	Best Case Gate Equivalent	Typical Gate Equivalent
PAL 16L8	16	8	56	8	368	184
PAL 16R4	16	8	60	4	400	200
PAL 16R6	16	8	62	6	410	205
PAL 16R8	16	8	64	8	424	212
PAL 20L8	20	8	56	8	376	188
PAL 20R4	20	8	60	4	400	200
PAL 20R6	20	8	62	6	410	205
PAL 20R8	20	8	64	8	424	212
FPLA 16 × 48 × 8	16	8	48	8	380	190
FPLS 16 × 48 × 8	16	8	48	8	540	270
FPLA 18 × 32 × 10	18	10	32	10	318	159
FPLS 16 × 32 × 12	16	12	32	12	456	228

Table 3. PLA Equivalent Gate Count for HCMOS Arrays

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